A Low-Cost Vectorless ATE-Channel Architecture for Testing High-Speed IO Signal Integrity in High Volume Manufacturing

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***Abstract* – The future manufacturing of SOCs at nanometer scale requires a radical change in the means and strategies to verify product quality while still keeping an economical balance between the cost to fabricate transistors and to test them. Since the ATE is no longer the only option to verify the correct manufacturing of silicon but built-in self test (BIST) solutions evolved to a powerful alternative, now the question appears: what will be suited better? However, instead of choosing either/or from alternatives our recommendation is to develop a combined solution-set towards an economical optimum that profits from synergy. This change in test philosophy is explained using the example of testing multiple multi-lane high speed IO (HSIO) interfaces in future SOCs.**

The testing of HSIO interfaces embedded into large digital SOC designs is still a huge technical and economical challenge. On-chip BIST combined with a loopback operation is a widely adopted alternative to costly ATE. However, it suffers the poor fault coverage of the high speed analog portion that significantly affects the product quality. The paper describes an ATE-channel architecture for vectorless testing of the analog content based on signal integrity measurements only, thus breaking the paradigm of vector support from an ATE. For at-speed functional verification, the concept relies on on-chip test content generation and compare thus forming a perfect synergy of what silicon and ATE can do best with the result of achieving an economical optimum for high volume testing.

Introduction

When VLSI was introduced it was a given that ATE is the means for functional verification to ensure product quality. Today we can recognize that the situation has radically changed. The complexity of silicon grew such dramatically that simple functional verification is no longer feasible. Scan based structural test methods that reconfigure the logic for testing purposes have displaced functional testing almost completely. These structural approaches are efficient for highly complex digital logic and offer an economic solution for high volume testing. However, since SOC devices get more and more heterogeneous significant portions of circuitry where no equivalent structural approaches exist will be embedded. Embedded RF and analog units as well as HSIO interfaces are examples. To achieve sufficient fault coverage on these blocks parametric testing in mission mode is still required. The mission mode related test requirements caused by those units are mainly responsible for driving test cost up into astronomical heights.

On the other hand the extremely high degree of integration possible on nanometer silicon reduced the cost of silicon space such that adding additional built-in self test (BIST) and design-for-test (DFT) related circuitry is no longer a cost issue. Combined with advances in the tooling environment this laid the fundament for automated BIST and DFT solutions that today are a highly attractive alternative to expensive mission mode oriented ATE.

The development of BIST and DFT techniques however, often assumed just simple and traditional ATE capabilities or even tried to avoid the ATE at all. The target of these strategies was to achieve sufficient fault coverage either by supporting structural approaches (logic BIST) or by simply providing on-chip pattern generation and compare for at-speed functional verification (HSIO BIST). On the other hand no major breakthrough is visible so far to deploy similar techniques to solve parametric test issues that particularly occur in heterogeneous SOC.

This situation suggests a change in the future development goals of ATE and BIST/DFT approaches. The target of each solution space should no longer be independent of each other creating a competing situation but should assume a synergetic coexistence. Pattern generation and compare for functional verification or support of structural test can naturally be done best and most economic by on-chip BIST/DFT circuitry. The ATE is still helpful for re-seeding the PRBS pattern generators or providing compressed ATPG stimulus for embedded deterministic test. For parametric verification of heterogeneous SOCs the ATE can hardly be replaced for accuracy reasons and due to missing flexibility of on-chip solutions. However, since parametric verification in most cases is done in functional mode, on-chip BIST can efficiently be used to assist the parametric verification by e.g. on-chip pattern generation and compare while the ATE

is doing the actual parametric measurement. This idea is explained in the following example of solving the test challenges for HSIO interfaces embedded in future SOC devices.

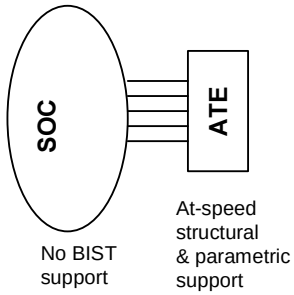

Fig. 1 Three ways to solve the test challenge in heterogeneous SOC

The example of testing HSIO interfaces

The historically grown perception related to ATE is the fact that at-speed functional as well as parametric timing or level verification can be done simultaneously in one shot on a per-pin basis. This is reflected in the architecture of ATE since its invention. A requirement for the ability to use this kind of ATE functionality for HSIO testing is that timing and level parameters can be precisely adjusted to marginal values within a bit interval and the high speed vector based test content can be stored in a per-pin memory for at-speed pattern generation, compare and error evaluation. The majority of today's ATE still show this type of architecture (fig. 2). Additionally it is also a wide spread business model that ATE is primarily developed for engineering which is the driver for performance and the technology is later leveraged to obtain a manufacturing solution. Different low cost packaging and assembly techniques for the pin-electronic channels as well as business models like pay-per-use are commonly used to meet the economical aspects in manufacturing and to guarantee the ROI for the ATE manufacturer.

With the upcoming HSIO interfaces however, the traditional ATE architecture ran into significant technical and economical issues and put the widely existing business model into question. With the HSIO interface standards crossing the Gigabit-per-second barrier, the signaling levels changed from of a few Volts to low voltage signals with a few hundred millivolts of differential amplitude. The timing specifications changed from assuming deterministic transitions with setup and hold times in the ns range to a statistical transition behavior that assumes deterministic and random jitter not to exceed a few ps while simultaneously reducing the available portion of the data eye by more than 50% to still guarantee a reliable data transmission on lossy links.

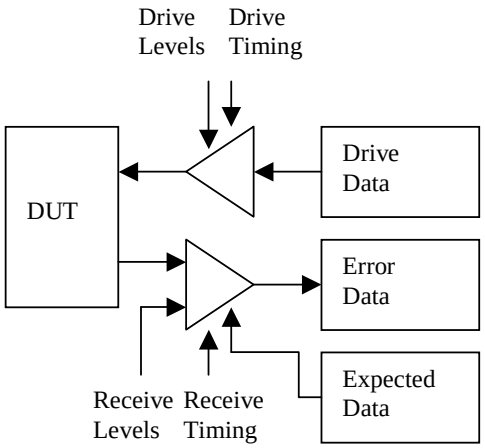

Fig. 2: Traditional ATE architecture combining parametric and functional verification

As a result the cost associated with handling the vector data at Gigabit-per-second data rates in the ATE with the appropriate timing and level accuracy to maintain test quality skyrocketed. The engineering tester proved to be completely inadequate to be leveraged or adapted to a respective manufacturing solution derivative.

Additionally, for the most advanced data rates reaching the 10Gbps mark the ATE companies had significantly difficulties to provide the traditional type of pin electronic channel timely enough in an fully integrated way with the expected pin density to support a massively parallel embedding of IO cells. Hooking up bench equipment like high-end bit error rate testers and ultra wideband scopes did neither meet the cost aspects on one hand nor the requirements for parallelism and system integration on the other hand. Therefore, ensuring the product quality in high volume manufacturing (HVM) for SOCs with embedded HSIO interfaces in an economically feasible way has become a nightmare and was listed as one of the most urgent ATE needs in the ITRS roadmap of 2001.

The advantage of making HSIO interfaces pervasive however, promised too much of an advantage from the system perspective, therefore the industry aggressively tried to solve the issues. Today we see two main trends. One trend was launched by the desperate IO cell designers who didn't get their circuitry tested on production ATE anymore. The design community began to add on-chip BIST circuitry into the IO cell that allowed at-speed functional verification by initially using PRBS data. The PRBS generation and compare BIST circuitry is switched alternatively to the internal parallel interface of the IO cell that operates in a loopback mode on the high speed side. In loopback mode the outbound data of the transmitter are simply fed back into the receiver at the high speed side. The symmetrical transceiver IO cell typically operates asynchronously on the transmit and receive side, greatly simplifying this concept (fig. 3).

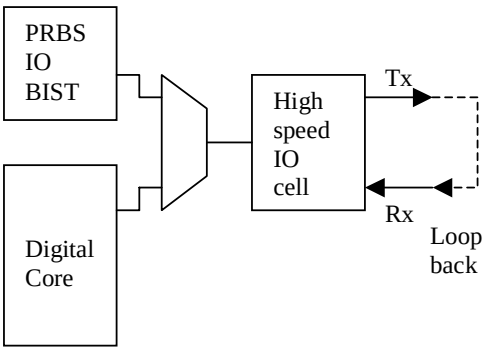

Fig. 3: Simple loopback testing of an HSIO cell by means of IO BIST.

The IO BIST test approach shows a couple of essential advantages. First of all the silicon overhead added is not much and when added to all IO cells of a massively parallel interface testing can be done in parallel on all pins simultaneously. Since a HSIO cell typically implements the physical layer of an high speed interface standard, the ATE challenge to setup the HSIO data according to the complicated individual PHY protocol including sophisticated line coding techniques and non-deterministic switching between control and payload information is avoided. The loopback path is inherently protocol transparent. A further significant advantage is that the actual technology in which a specific IO cell is implemented is used also for testing, this is independent from the ability of ATE to provide test solutions at the same leading edge data rates in time. And finally the designers provide the test content and assure the fault coverage. No test engineers are needed to convert and correlate simulation data to test vectors and to provide a respective portion for the test program in time.

However, IO BIST also shows some significant disadvantages. Since it interfaces only at the parallel side of the IO cell, the on-chip BIST is neither able to verify DC parameters nor the parametric performance related to signal integrity. Signal integrity however, is one of the fundamental requirements for high speed transmission and is significantly affected by process variation and design robustness issues, such as supply noise crosstalk, that hardly can be verified by simulation. Most of the HSIO cell designs squeeze the process technology to the limit to achieve the highest data rates for competitive reasons thus loosing the process margins for signal integrity and exposing the manufacturing to yield issues. Designers of high end network switches for example, who are already embedding more than 128 high speed serial links running at up to 3.125Gbps into their SOCs, frankly admit that they can't ensure product quality without parametric testing of jitter in production.

As a second trend the ATE companies tried to react with new products only accepted with reluctance so far, due to cost. To lead the technological progress in the high speed interfaces with the timely development of pin electronic channels that can handle the vector generation and compare at-speed is a great technological challenge. Therefore, the solutions generated mostly used multiplexing techniques to double the speed of existing pin modules. Some solutions were even created with active multiplexing on the loadboard causing correlation and reliability issues in manufacturing. A generic issue of the multiplexed solution is the reduction in pin density because the two pin modules and the multiplexer eat up a lot of space inside the testhead and increase the cost significantly. The value however, that is added by well performing and highly integrated ATE solutions is the important support of signal integrity testing such as jitter and at speed signal level performance. The correctness of these parameters is absolutely essential for ensuring the product quality and the compliance to the key standards.

Therefore, it is becoming more and more obvious that neither the DFT approaches providing on-chip BIST solutions nor the ATE industry providing support for the crucial signal integrity are able to solve the economical problem alone while simultaneously providing enough fault coverage for the HSIO interfaces in today's leading edge SOC silicon.

Proposal for a new ATE channel architecture

1. General Approach for a vectorless ATE channel

As in many other domains an optimal solution can't be achieved by a single solution component. On the other hand when combining two solution components in a smart and sophisticated way synergy can be obtained that frees an additional cost reduction potential not available from both contributors alone. In a generic perspective the proposal means to combine on-chip BIST techniques with ATE capabilities: The on-chip BIST implements what it can do best and where the ATE would be a solution too costly for HVM; the ATE is doing what it can do best with off chip instrumentation and where an on-chip BIST solution has difficulties to reach the required performance or is too difficult for a timely implementation, verification and correlation, also taking into account time-to-market aspects of the final product.

For the high speed serial interfaces technology that was developed years ago mainly for telecom applications we already saw such a synergistic approach for the system level tests on the bench. The measurement equipment manufacturers developed the bit error rate tester (BERT) focused to ensure the correctness of the data content as well as the concept of the eye diagram measurements that ignores the data content and just focuses to signal integrity. Both together were used as an ideal combination to ensure product quality for the physical layer devices of key communication standards such as SONET or IEEE 802.3 Ethernet up to 10Gbps.

In the same way the proposed solution separates between the task to verify the data content from the task to verify signal integrity. Providing the test content at the required data rates can be done pretty economically with on-chip BIST circuitry and can be tested in a protocol transparent way in loopback mode. In contrary the ATE contributes with the required performance to allow signal integrity measurements hardly to achieve in a timely and accurate enough way with on-chip circuitry. When we combine both we'll get a lot of synergy for test cost savings.

What is important however, this approach breaks the key paradigm that the ATE has to provide vectors and vector handling at speed. It also breaks the paradigm that the ATE is able to do timing and functional verification simultaneously. This is exactly what makes the ATE channel costly and what is avoided with the proposed approach. Providing test content on-chip is cheap for today's CMOS technologies and can be added with only minimal overhead in design time and silicon space. However, it requires that the designer fully takes care of the test content required not only for functional verification of the device to correctly transmit the payload but also to provide the test content for the right parametric testing of signal integrity parameters on the ATE by means of killer pattern tweaked for maximum stress to the PLLs in terms of data dependent jitter or with respect to standard compliance criteria. The ATE in turn extends the idea of the loop. It extends the external loopback path into low cost loopback channel cards that allow the pattern independent measurement of signal integrity parameters and optionally gives additional access to DC measurement resources. This loopback channel card is inherently low cost because it does not contain those costly elements that allow high speed vector handling such as a test processor or vector memory.

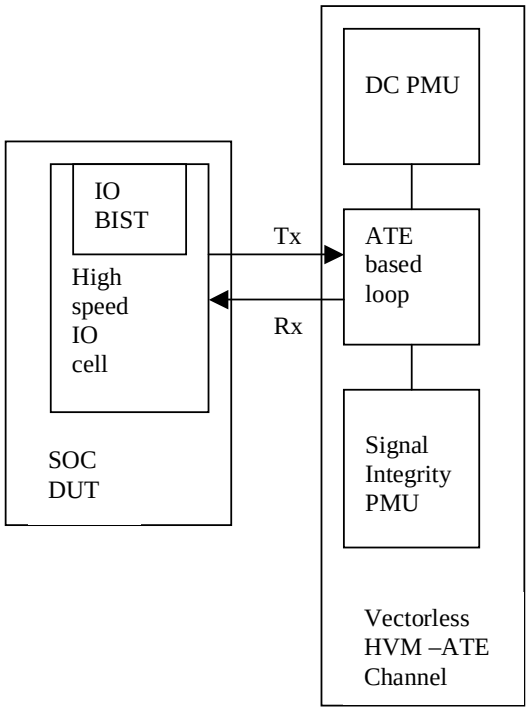

Fig. 4: Generic approach of the proposed vectorless ATE channel architecture

The setup on the ATE for the parametric measurements does not require any vectors, the proposed method therefore is called vectorless parametric testing. The parameters tested to verify the signal integrity depend on the production test

needs of the specific application and can be as simple as just measuring jitter generation and tolerance or receiver sensitivity. Or it could be more sophisticated parameters to also include more complex aspects e.g. like data to clock skew.

2. Options for implementation

Already with the standardization of the IEEE 802.3 10/100BASE-T physical layer standard the standardizing authority recognized the issue of signal integrity when transmitting 100Mbps on 100m of twisted pair cables and therefore included a so called “line equivalent filter” as a test requirement in the standard. The filter was an implementation using passive discrete parts and tried to approximate best the essential behavior of the lossy line with respect to signal integrity. In [1,2] we leveraged the concept for low cost production testing of SerDes operating in loopback mode. This can be seen as the most simple way to implement the proposed approach (fig. 5).

The implementation described in [1,2] was particularly meant to test the number 1 quality issue of HSIO interfaces that is jitter. It was therefore called jitter injection module (JIM). The deployed test methodology assumed that jitter generation in the transmitter as well as jitter tolerance is tested simultaneously. The JIM was designed to add that much of jitter that gets marginal when adding the allowed jitter generation and an additional guardband. Therefore when the transmitter generates excessive jitter the test fails in the same way as it fails when the receiver does not show up with the appropriate jitter tolerance.

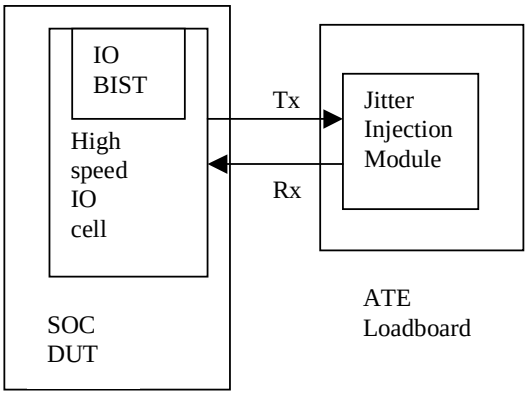

Fig. 5: Simple approach to implement vectorless testing of signal integrity using a jitter injection module

However, the JIMs have the key disadvantage, that the amount of jitter that gets intentionally injected into the loop is dependent on the data rate. Therefore IO cells that operate at different data rates can only be tested for a single data rate and the JIM must be provided in an application specific way.

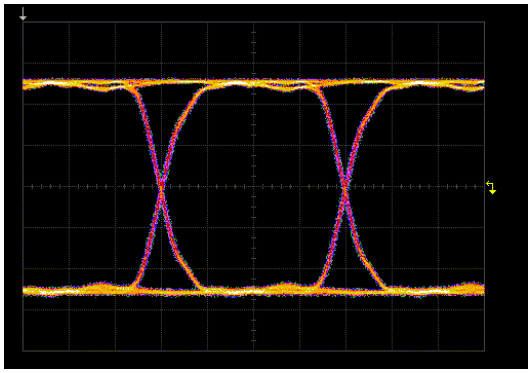

Fig. 6a: Transmitter Output

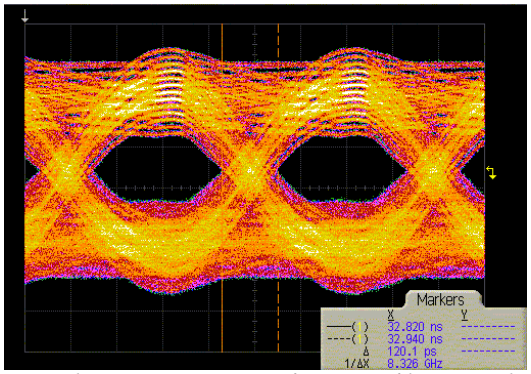

Fig. 6b: Receiver input after JIM filtering. The receiver must tolerate the line equivalent eye closure to pass the parametric test.

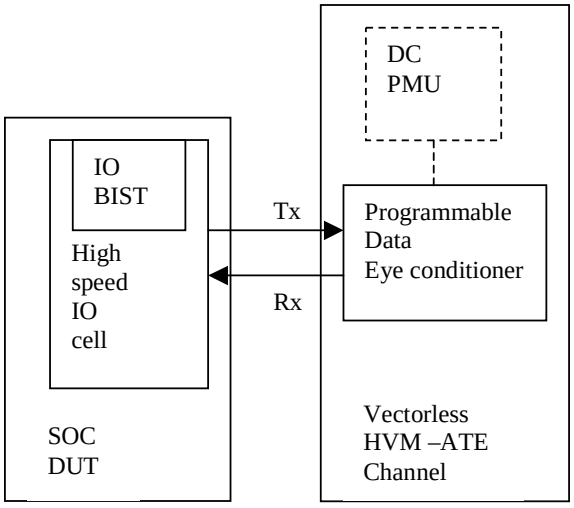

Fig. 7: A more flexible approach for loopback testing using a data eye conditioner for independent jitter and level adjustment in a vectorless ATE channel

From the already published JIM idea a more flexible implementation can be derived. This implementation not only makes the JIM tunable but also allows re-adjusting the levels independent from jitter injection. Therefore the user has the option to precisely condition the transmitter data eye to test the transceiver for jitter and level performance simultaneously. Since this flexibility can't be achieved by passive components on the loadboard only the more flexible solution requires a dedicated loopback card with the option for the user to program it using the ATE software. Optionally DC access to the high speed loop could be provided to additionally allow DC measurements if this turns out to be a really important HVM requirement.

Economical Aspects

Looking at the cost savings potential the material cost break down shows that the cost of active silicon including the vector memory is about 50% of the total cost of a pin electronic channel that would be able to address most of the current HSIO standards in a traditional way allowing functional verification as well as parametric measurements for signal integrity (fig. 8). Even though the material cost does not allow a direct mapping to the final selling price of a product a significant cost reduction for the user becomes visible.

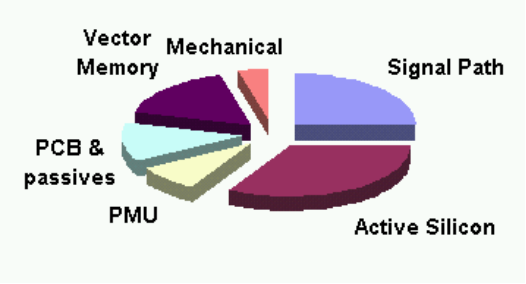

Fig. 8 Material cost break down of a traditional HSIO channel.

The other indicator of significant cost reduction potential is visible on the side of the engineering cost for the proposed architecture. For a traditional pin electronic the amount of investments in engineering for testprocessor and vector memory / vector handling is about 50% of the hardware and about 65% of the software investments. A vectorless architecture that does not contain a test processor and no vector memory not only halves the hardware development cost but dramatically cuts down the cost for software engineering by more than 50%. Thus it is out of question that a vectorless architecture combined with on-chip pattern generation and compare will free a tremendous amount of synergy for cost reduction in HVM.

In case an ATE manufacturer adopts the proposed architecture as a main contribution to make production testing of HSIO interfaces economically feasible another important financial consequence should not be neglected. The traditional ATE business models assumed that the fundamental architecture of the pin electronic channel is the same for engineering as well as for HVM. The ROI calculation to justify the development of a new product covering higher data rates for example assumed to generate the return dominantly from the volume sales into the HVM market.

Meanwhile a new trend seems to be visible. In order to meet the economical goals of the HVM market dedicated products matching the on-chip DFT approaches are required, totally differing in architecture from what is needed for engineering and characterization. The proposed vectorless pin electronic architecture is just an example for this much more generic trend. On the other hand lowest cost production seems to be only feasible from the semiconductor manufacturers point of view when a more thorough characterization and design validation is performed that ensures the compliance with the HSIO standards as well as the appropriate design robustness versus the process variations. A common fact is today that about 75% of the overall characterization and validation time is spent solely for determining the signal integrity performance.

This in turn requires better and more costly ATE solutions to characterize and validate SOCs with embedded HSIO interfaces in engineering. Now the traditional business model of an ATE manufacturer fails because the ROI has to be taken from the engineering business only, the HVM business uses a different low-cost architecture developed separately. This puts the development of a dedicated engineering solution into question despite the fact that the equipment cost in engineering is less critical than in HVM. Other ways have to be found to avoid that engineering ATE becomes the roadblock for HSIO interfaces and breaks Moore's law on the economical side.

One option to solve these issues caused by the architectural split is to make re-use of developments for bench equipment components. Since bench equipment is typically developed earlier than ATE and uses the most advanced technologies for ultimate performance sharing these component developments between ATE and bench equipment also guarantees the timely availability of high-end engineering solutions. A key requirement is that the bench equipment component development takes the ATE re-use into account to support a high degree of parallelism, ATE-like throughput as well as component interfaces that fit to the ATE platform architecture. Since today bench equipment is available to test particularly the signal integrity parameters as well as the bit error rate related functionality up to 40Gbps this seems to be the way of choice for future engineering

solutions complementing the proposed vectorless architecture for HVM.

Summary

By extending the loopback path into a vectorless pin electronic channel card we were able to define an ATE architecture that meets the goals of economic testing of HSIO interfaces in production. The proposed approach however requires breaking the paradigm that an ATE provides vector support. Instead this architecture essentially relies on on-chip BIST as a key DFT contribution. The well-balanced combination of vectorless signal integrity testing using accurate ATE to ensure fault coverage for the analog IO cell portions and the low cost on-chip BIST running in loopback mode to allow at-speed functional verification of the digital transmission generates significant amounts of synergy that in turn creates a huge potential for cost saving. The achieved synergy between DFT and ATE therefore allows reaching the economical goals for HVM.

We have also shown that choosing a fundamentally different architecture for HVM than for engineering does not create a roadblock for engineering solutions. The suggested way to go for the future in engineering is the re-use of bench equipment components developed early with new upcoming high speed waves. The key learning is that these components must take the ATE re-use into account already during their initial development.

Literature

[1] Bernd Laquai, Yi Cai: Testing Gigabit Multilane SerDes Interfaces with Passive Jitter Injection Filters, IEEE Proc. of the International Test Conference 2001

[2] Yi Cai, Bernd Laquai, Kent Luehman: Jitter Testing for Gigabit Serial Communication Transceivers, IEEE Design and Test of Computers, Jan-Feb 2002